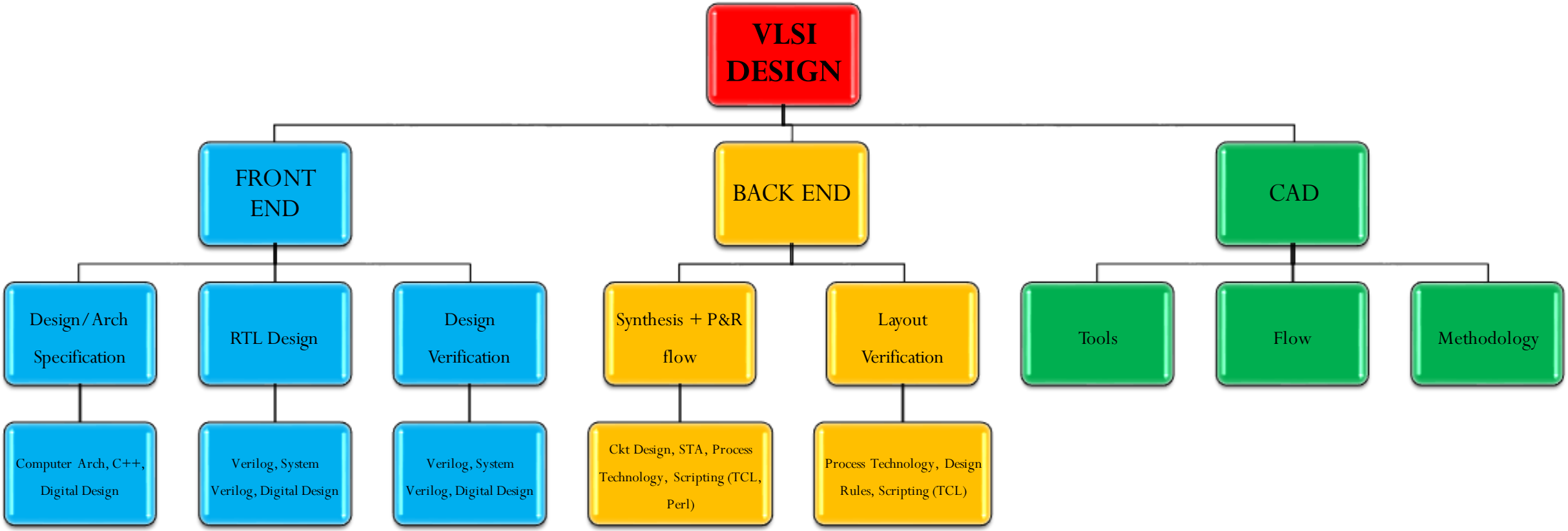
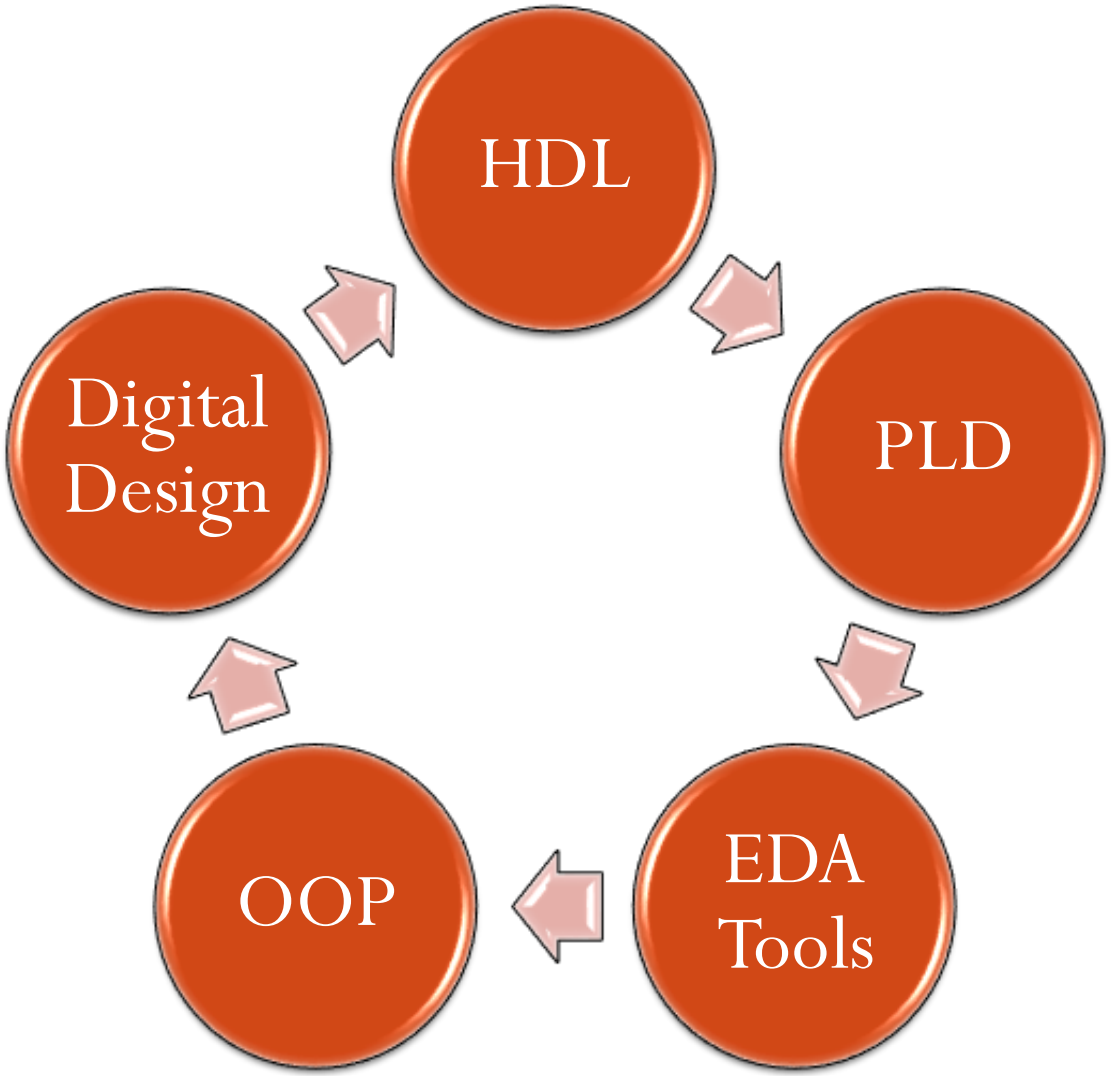
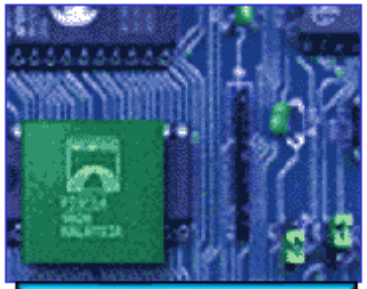
VLSI Design – An Overview

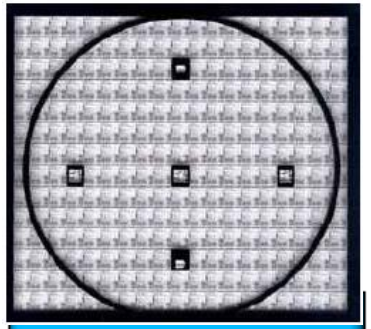



HDL
PLD
EDA Tools
OOP
Digital Design

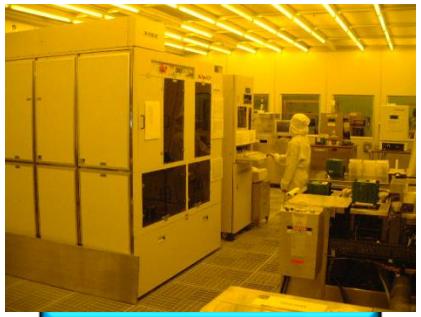
Major Industry Components



Design Services

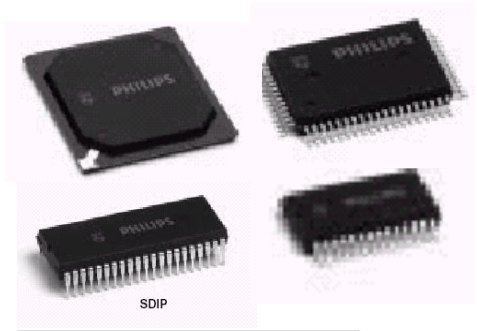


Mask Making



Wafer Manufacturing

Wafer Test



Assembly & Final Test

Market Trends

- Companies
  - Product based
  - Service based
- Designer to Verification Engineers Ratio
- Increase in demand with complexity due to data boom

Learning Outcomes

- Verification….why, how and what?
- Verification options, methodologies, approaches and plan
- Test Bench Fundamentals
- Writing your SystemVerilog code
- Various SystemVerilog Data Types including User Defined Data Types
- Procedural Statements and Flow Control Statements
- Interface Concepts
- Examples to practice on verification tool EDA Playground

Verification Engineer Skillset

- Language knowledge of
  - System Verilog, UVM
  - System Verilog Assertions (Formal + Simulation)
  - VHDL (preferred for Designs)
- Digital Design and Computer Architecture Concepts
- Knowledge of Industry Standard Protocols like AXI, HDMI, PCI, USB
- Knowledge of Processors, System On Chip, FPGAs, Caches, Memories.
- Tools used for Debug Experience :
  - Cadence : NCSIM, IEV
  - Synopsys : VCS(Verdi) , Jasper
- Code Repository Systems like Perforce, CVS, ClearCase
- Scripting languages like Perl, Python

Web References

- https://www.chipverify.com
- https://testbench.in
- http://www.asicguru.com
- http://www.asic-world.com
- https://verificationguide.com/