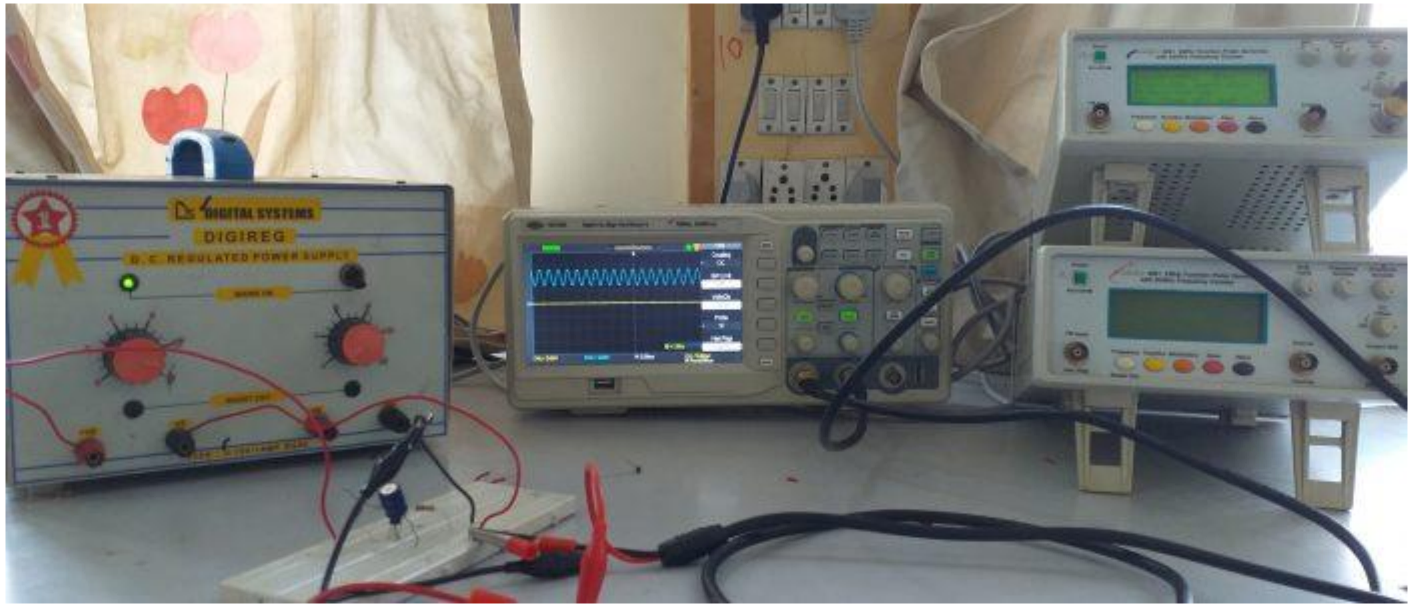
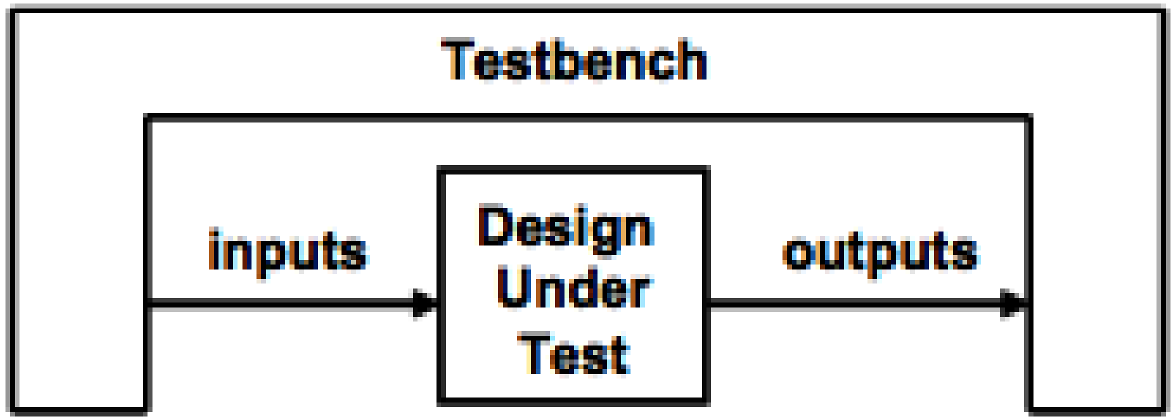
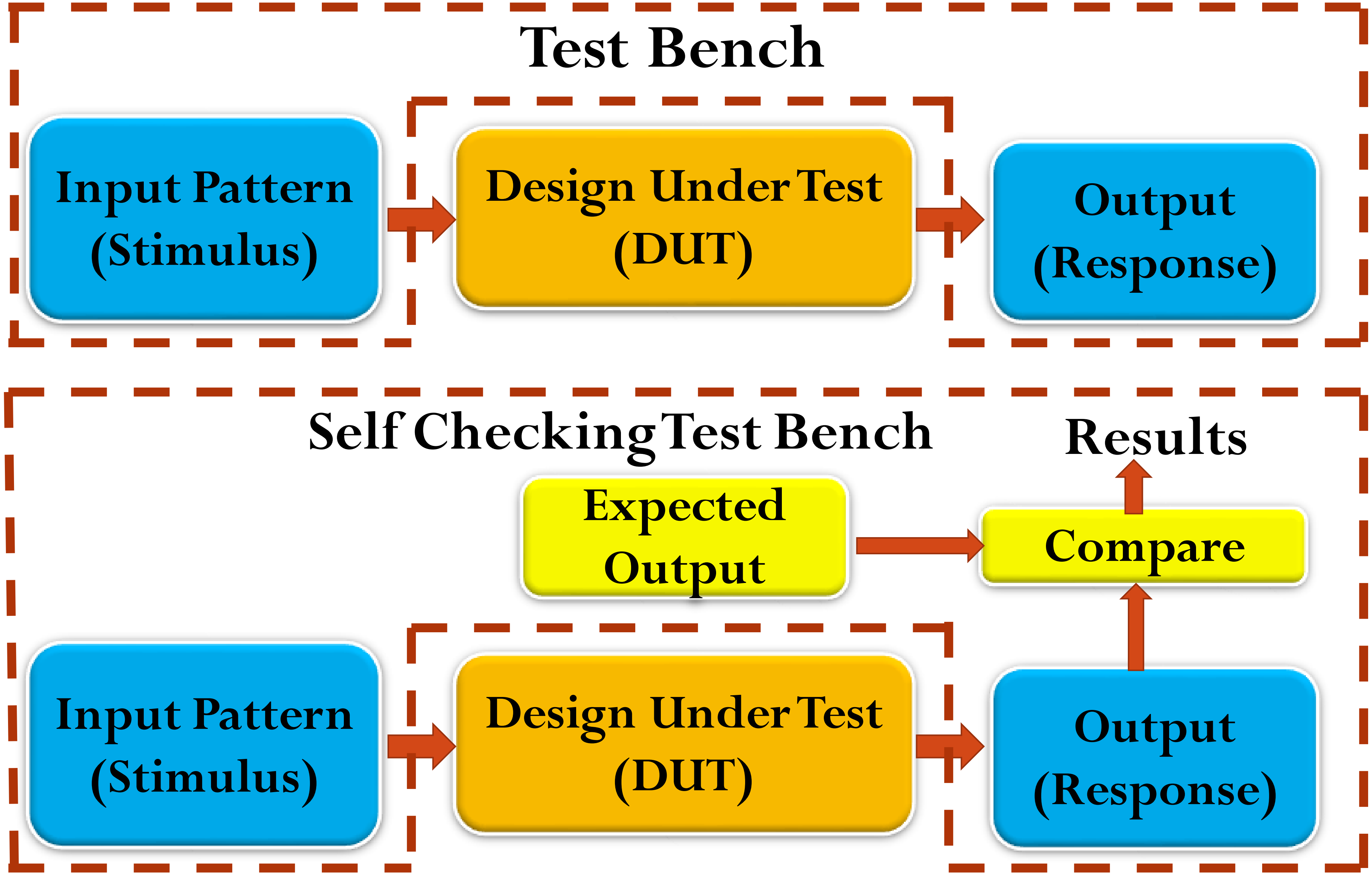
Basic TestBench Functionality



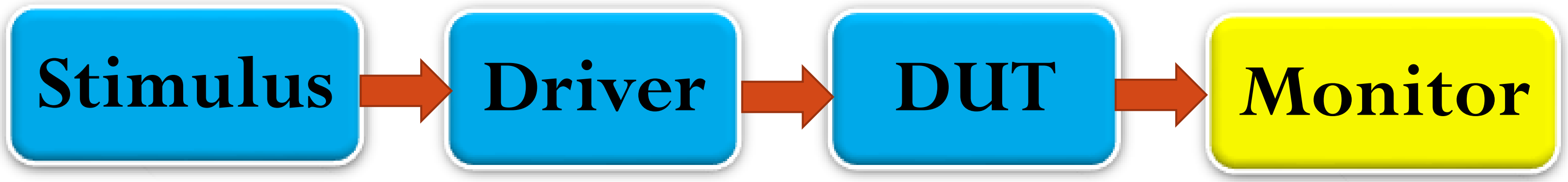


BasicTestBench Functionality

1. Generate stimulus
2. Apply stimulus to DUT
3. Capture the responses
4. Check for correctness
5. Measure progress

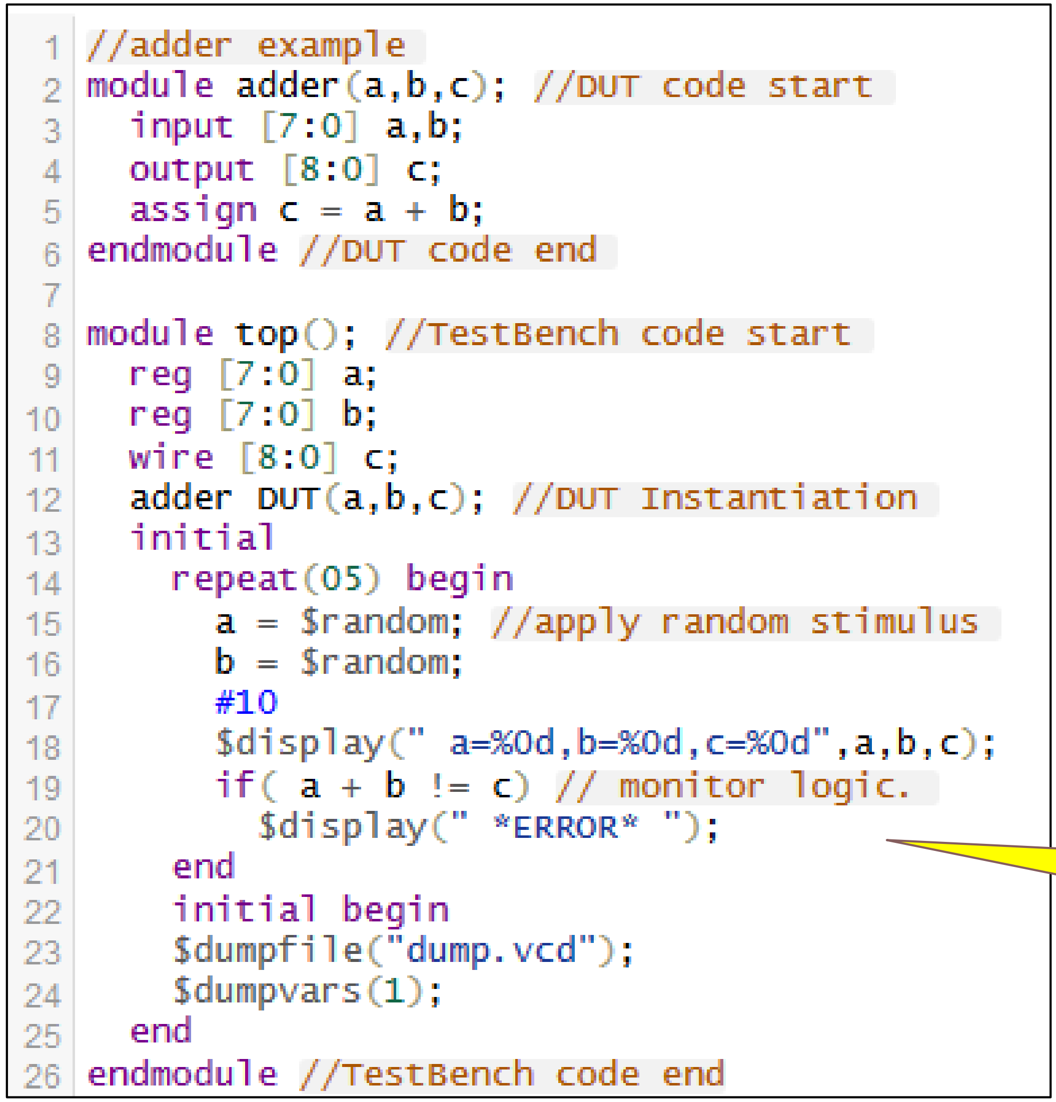

Test Bench
Input Pattern (Stimulus)
Design Under Test (DUT)
Output (Response)
Self Checking Test Bench
Results
Expected Output
Compare
Input Pattern (Stimulus)
Design Under Test (DUT)
Output (Response)

Self Checking Testbench



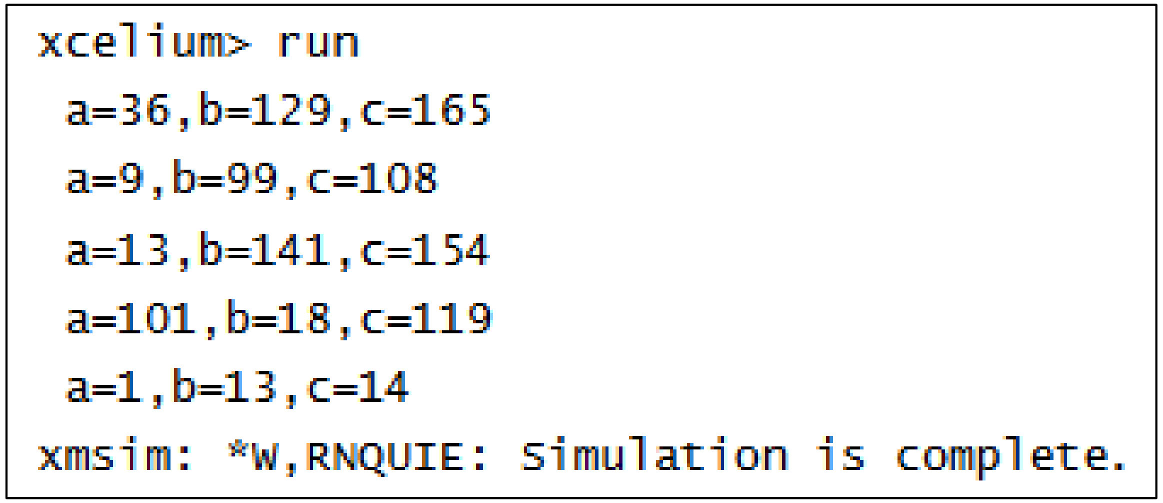
- Require considerably more effort during the initial test bench creation phase
- This technique can dramatically reduce the amount of effort needed to re-check a design after a change has been made to the DUT.
- Debugging time is significantly shortened by useful error-tracking information that can be built into the TestBench to show where a design fails.

Self Checking Testbench



```verilog
//adder example
module adder(a,b,c); //DUT code start
  input [7:0] a,b;
  output [8:0] c;
  assign c = a + b;
endmodule //DUT code end

module top(); //TestBench code start
  reg [7:0] a;
  reg [7:0] b;
  wire [8:0] c;
  adder DUT(a,b,c); //DUT Instantiation
  initial
    repeat(05) begin
      a = $random; //apply random stimulus
      b = $random;
      #10
      $display(" a=%0d,b=%0d,c=%0d",a,b,c);
      if( a + b != c) // monitor logic.
        $display(" *ERROR* ");
    end
    initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
endmodule //TestBench code end
```



```
xcelium> run
 a=36,b=129,c=165
 a=9,b=99,c=108
 a=13,b=141,c=154
 a=101,b=18,c=119
 a=1,b=13,c=14
xmsim: *W,RNQUIE: Simulation is complete.
```

Self checking

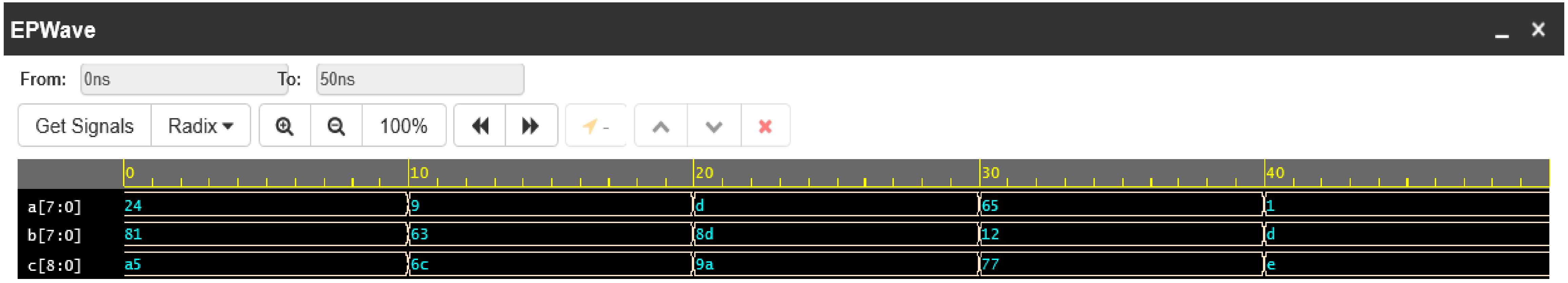
Techniques for Testbench Creation

- **Testbench in HDL** (smaller designs)
- **Testbench in Programmable Language Interface (PLI)**
- **Waveform-based**
- **Transaction-based**
- **Specification-based**

How to Check Results

How does a Verification engineer check whether the results obtained from the simulation match the original specification of the design?

1. output is displayed in waveform window OR
2. messages are sent to terminal for visual checking.



From: 0ns To: 50ns